Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A method of manufacturing an electronic device including a thin film transistor, comprising the steps of:

(a) forming a gate structure including forming a gate electrode on an insulating surface;

(b) depositing an insulating layer over the gate electrode and a region adjacent an edge of the gate electrode, such that the insulating layer comprises two first outer surfaces which are substantially parallel to, and mutually spaced normally of, the insulating surface with a step extending therebetween, said step forming a second outer surface forming an angle relative to said first two outer surfaces;

(c) depositing a layer of semiconductor material on said first and second outer surfaces;

(d) depositing a layer of electrode material on said first and second outer surfaces;

(e) depositing a layer of negative resist material over the electrode material layer formed in step (e), the resist material being soluble in a predetermined solvent;

(f) irradiating the resist layer using a beam at a predetermined angle, the surface of the resist overlying said two first outer surfaces being exposed more by said beam than the surface of the resist overlying the second outer surface due to said angle formed by said two first outer surfaces relative to said second outer surface, to render more exposed portions insoluble in the predetermined solvent, the portion overlying the step being insufficiently exposed such that it remains soluble, without the use of a mask to selectively block radiation from said reaching said portion overlying the step;

(g) developing the resist layer using the predetermined solvent, thereby removing the portion overlying the step; and

(h) removing the portion of the electrode material layer exposed by step (g) to define source and drain electrodes which extend over a respective one of the outer surfaces of the insulating layer to the step.

2. (Original) A method of claim 1 wherein step (c) of depositing the semiconductor layer is carried out after step (h).

3. (Original) A method of claim 1 wherein the edge of the gate electrode is substantially normal to the insulating surface.

4. (Original) A method of claim 1 wherein a second thin film transistor is formed simultaneously with the first thin film transistor at an opposing edge of the gate electrode.

5. (Original) A method of claim 1 wherein a low definition process is used to define one or more of the gate electrode and the layers.

6. (Original) A method of claim 5 wherein a low definition process is used to define the gate electrode and the layers.

7. (Original) A method of claim 1 wherein the semiconductor material comprises an organic material.

8. (Original) A method of claim 1 wherein the height of the upper surface of the gate electrode above the substrate is in the range of 0.05 to 1.5 microns.

9. (Original) A method of claim 1 including a further step after step (g) and before step (h) of subjecting the resist layer to a reflow process.

10. (Original) A method of claim 1 including a further step after step (g) and before step (h) of subjecting the resist layer to an ashing process.

11. (New) A method of manufacturing an electronic device including a thin film transistor, comprising the steps of:

forming a first gate structure on an insulating surface, said gate structure having non-parallel first and second faces, said first gate structure having an outer layer;

forming a resist layer on said first gate structure such that said resist layer has non-parallel first and second faces overlying said gate structure first and second faces;

irradiating said resist layer first and second faces from a direction and for a time interval such that said resist layer first face receives more radiation than said second face as a result of differing angles of incidence of radiation, such that the difference between the radiation received by said resist layer first and second faces causes a solubility property of said resist layer first and second faces to be different;

developing to remove a portion of a one of said resist layer first and second faces rendered more soluble in said step of irradiating to expose an underlying portion of said gate structure outer layer without removing a portion of another of said resist layer first and second faces rendered less soluble in said step of irradiating.

12. (New) The method of claim 11, further comprising the step of removing at least a portion said underlying portion to expose a portion of said gate structure outer layer.

13. (New) The method of claim 11, wherein said resist layer is of negative resist material and said one of said resist layer first and second faces rendered more soluble in said step of irradiating includes said resist layer first face.

14. (New) The method of claim 11, wherein said gate structure outer layer includes a layer of electrode material.

15. (New) The method of claim 11, wherein said non-parallel first and second faces are substantially perpendicular.

16. (New) The method of claim 11, wherein said step of irradiating includes irradiating with a beam having a substantially uniform direction of radiation.

17. (New) A method of manufacturing an electronic device including a thin film transistor, comprising the steps of:

forming structures on a substrate, each of said structures having at least one terminal portion;

depositing a resist layer on said structures;

irradiating said resist layer with a beam;

developing said resist to remove a first portion thereof to expose said at least one terminal portion of each of said structures underlying said first portions;

said steps of forming, depositing, and irradiating being such that said beam is incident on said first portions at first angles of incidence and on second portions of said resist layer at second angles of incidence such that said first portions receive a different amount of radiation than said second portions, said different amount causing said first portions to removed in said step of developing and causing said second portions to not be entirely removed in said step of developing, whereby selective regions of a resist are irradiated at least partly without the use of a separate mask.

18. (New) The method of claim 17, wherein said step of irradiating includes irradiating with a beam having a uniform direction of radiation and a difference in said first and second angles of incidence results from a difference in angles of surfaces of said first and second portions relative to a plane of said substrate.

19. (New) The method of claim 17, wherein said structure includes a gate.

20. (New) The method of claim 17, wherein said step of depositing includes depositing said resist layer such that it has at least two outer surfaces which are substantially non-parallel.